MC48 General Information

Max Hailperin; Fall, 1995

Outline

MC48 will cover the architecture and organization of computer hardware. We will look at the MIPS architecture as a representative modern RISC architecture, and do some assembly language programming for that architecture. We'll see how numbers are represented within a computer and how the circuits that perform arithmetic operations on those numerals are organized. With a high-level overview of digital logic design to support us, we'll look at how the datapaths and control circuits of processors are designed, and in particular we'll look in some depth at pipelined processor design, which is the key organizational principle at work in most present-day processors. We'll examine the use of memory hierarchy (cache memory and virtual memory) to provide the illusion of a large fast memory from the reality of limited fast memory plus a larger but slower memory. We'll look at input/output devices and buses, and at parallel computers. Throughout the course there will be an emphasis on the quantitative performance characteristics of computer systems; we'll look at the influence of architecture and organization on performance, and take an introductory look at the empirical and analytical tools appropriate to the study of performance. Performance measurement will be one of the main themes reinforced through the lab assignments; the other will be assembly language programming.

Office Hours

I will be available in my office (OHS 303) on Tuesdays and Thursdays from 9:00 to 9:50, on Mondays and Wednesdays from 3:30 to 4:20, and by appointment. You may send me electronic mail at max@gac.edu or call me at extension 7466.

Text

Our text will be the *Computer Organization and Design: The Hardware/Software Interface* by David A. Patterson and John L. Hennessy, Morgan Kaufmann, 1994.

Labs

We'll have lab sessions on Tuesdays, in OHS 326. (We'll meet in the scheduled classroom, OHS 320, on the other four days: Monday, Wednesday, Thursday, and Friday.) The labs are shown in the syllabus. Lab 0 the first Tuesday and Lab 5 the last Tuesday are special one-day experiences that don't involve written lab reports. The other four labs will involve writing a report; the due dates are shown in the syllabus, in the same column as the homework due dates.

Tests

Their will be two in-class tests during the semester, which are indicated in the syllabus, and a final exam scheduled by the registrar. The tests will be open book and open notes, and may include problems from the book.

Honor

Students are encouraged to discuss the course, including issues raised by the assignments. However, the solutions to assignments should be individual original work unless otherwise specified. If an assignment makes you realize you don't understand the material, ask a fellow student a question designed to improve your understanding, *not* one designed to get the assignment done. To do otherwise is to cheat yourself out of understanding, as well as to be intolerably dishonorable.

Any substantive contribution to your solution by another person or taken from a publication should be properly acknowledged in writing. Failure to do so is plagiarism and will necessitate disciplinary action.

Late Assignments

All homework and lab assignments are due at the beginning of class on the day indicated. Late assignments will be penalized by one letter grade for each weekday late or fraction thereof. However, no late assignments will be accepted after graded assignments are handed back.

If you are too sick to complete an assignment on time, you will not be penalized. Simply write "late due to illness" at the top of the assignment, sign your name and hand it in. Other circumstances will be evaluated on a case-by-case basis.

Grade Changes

Please point out any arithmetic or clerical error I make in grading, and I will gladly fix it. You may also request reconsideration if I have been especially unjust.

Grading

I will provide you with a letter grade on each homework and lab assignment and on each test, in addition to the mid-term and final grades, so that you may keep track of your performance. As a guideline, the course components will contribute to your final grade in the proportions indicated below:

homework	40%	(8 assignments, 5% each)
lab reports	20%	(4 assignments, 5% each)
intra-term tests	20%	(2 tests, 10% each)
final exam	20%	

However, I reserve the right to subjectively adjust your final grade. Please see me if you have any question how you stand. Class participation is not graded; however, it allows you to find and repair the gaps in your understanding before doing the assignments, and thus can dramatically improve your grade.

Style Guidelines

All homework and lab reports should be readily readable, and should not presuppose that I already know what you are trying to say. In particular:

- Use full English sentences where appropriate (namely almost everywhere, including in mathematical proofs or derivations).

- Word-process or type your homework if you can. In any case, make sure it is legible.
- Use diagrams, tables, programs, and calculations as supporting components of English writing, not in isolation. Remember that your goal is to communicate clearly, and that the appearance of these technical items plays a role in this communication process.

Be sure your assignments are always stapled together and that your name is always on them.

Accessibility

Please contact me immediately if you have special physical circumstances, e.g. impaired vision, which may affect the accessibility of any course components. I will do my best to facilitate necessary arrangements or resources.

Syllabus

In the reading column, a single number with no decimal point indicates an entire chapter. A reading indicated as terminating on a particular page number means to read up to the heading on that page; this heading may be at the top of the page, in which case the reading doesn't actually include any of the material on that page.

This is my best guess as to the rate at which we will cover material. However, don't be shocked if I have to pass out one or more revised syllabi.

Date	Reading	Topic	Due
9/6		Introduction	
9/7	1	Computer abstractions and technologies	
9/8	2.1–2.4	Performance measurement	
9/11	2.5–2.9 and handout	Performance (continued) and C	
9/12		Lab 0: Under the hood (no report)	
9/13	3.1–3.5	Instructions	HW 1
9/14	3.6–3.8	More on instructions	
9/15	3.9–3.14	Assembly language programming	
9/18	A.1–A.6	More on assembly language programming	
9/19		Lab 1: Elementary assembly language programming	
9/20	4.1–4.3	Addition and subtraction	HW 2
9/21	4.4–4.5	An Arithmetic Logic Unit	
9/22	4.6	Multiplication	
9/25	4.7	Division	
9/26		Lab 1 (continued)	
9/27	4.8–4.11	Floating point arithmetic	HW 3
9/28	B.1–B.3	Combinational logic	
9/29	B.4–B.6	Sequential logic	
10/2		Review/catch-up	
10/5		Test 1	
10/6	5.1–5.2	Processor datapaths	
10/9	5.3–p. 306	Single-cycle processor	
10/10		Lab 1 (concludes)	
10/11	5.3 (rest)	More on single-cycle processor	
10/12	5.4	Multi-cycle processor	Lab 1
10/13		More on multi-cycle processor	
10/16	5.5–5.9	Microprogramming	
10/17		Lab 2: More advanced assembly language programming	
10/18	C.1–C.3	Mapping control to hardware	
10/19		Review/catch-up	HW 4

Date	Reading	Topic	Due
10/24		Lab 2 (continued)	
10/25	6.1–6.2	Pipelined datapath	
10/26		More on pipelined datapath	
10/27	6.3	Pipelined control	
10/30	6.4	Data hazards	HW 5
10/31		Lab 2 (concludes)	
11/1	6.5	Stalls	
11/2		More on stalls	Lab 2
11/3	6.6	Forwarding	
11/6	6.7–6.8	Control hazards	
11/7		Lab 3: Measuring instruction set usage	
11/8	6.9–6.12	More on pipelining	
11/9		Review/catch-up	
11/10		Test 2	
11/13	7.1–7.2, p. 469	Caches	
11/14		Lab 3 (concludes)	
11/15	7.2 (rest)	More on caches	
11/16	7.3	Virtual memory	Lab 3
11/17		More on virtual memory	
11/20	7.4–7.7	Memory hierarchy analysis	
11/21		Lab 4: cache simulation	
11/22		Review/catch-up	HW 6
11/27	8.1–8.3	Input/output devices	
11/28		Lab 4 (concludes)	
11/29	8.4	Buses	
11/30	8.5	Input/output interfacing	Lab 4
12/1	8.6–8.8	More on input/output	
12/4	9.1–9.4	Parallel programming	HW 7
12/5		Lab 5: Parallelism on networked workstations (no report)	
12/6	9.5	Bus-based MIMD architectures	
12/7	9.6–9.10	Network-based MIMD architectures	
12/8		Review/catch-up/evaluation	HW 8