MCS-284 Final Exam

Serial #:

This exam is closed-book and mostly closed-notes. You may, however, use three 8 1/2 by 11 sheets of paper with *hand-written* notes for reference. (Both sides of the sheets are OK.)

Please write your name only on this page. Do not turn the page until instructed, in order that everyone may have the same time. Then, be sure to look at all problems before deciding which one to do first. Some problems are easier than others, so plan your time accordingly. You have 120 minutes to work.

Write the answer to each problem on the page on which that problem appears. You may also request additional paper, which should be labeled with your test number and the problem number.

If you are stuck, ask for help. At worst, I'll offer to sell you a hint for some points.

Name: _____

Problem	Page	Possible	Score
1	2	12	
2	3	12	
3	4	12	
4	5	12	
5	6	12	
Total		60	

1. [**12 Points**] For both parts, you only *need* to show the final answer, but will only receive partial credit for a wrong answer if you show your work.

   (a) Write in binary the single-precision (i.e., 32-bit) floating-point number representing $-9/32$.

   (b) Add the following two single-precision floating-point numbers, showing your result in binary as a single-precision (32-bit) floating-point number. Note that these numbers are divided into chunks of four bits just to help you count positions more accurately. The chunks do not correspond to the logically significant portions of the representation.

   ```
   0101 0101 0101 0000 0000 0000 0000 0000
   0101 0100 0000 0000 0000 0000 0000 0000
   ```

2. [**12 Points**] Consider a direct-mapped cache with a total capacity of 16 words and a block size of two words. Assume the cache is initially empty and that we are using word addresses (as in the homework), so that words have addresses 0, 1, 2, etc. For the following sequence of addresses, indicate which are misses and which are hits. Also show which addresses (if any) are contained in each location of the cache at the end. (To receive partial credit for an incorrect answer, you should also show your work, including in particular how the cache contents evolves, e.g., by crossing out addresses that are replaced.)

   `0 5 10 20 31 10 5 1`

3. [**12 Points**] Compare three caches, each of which can hold 4KB worth of data:

   - C0 is direct-mapped and has one-word blocks.
   - C1 is direct-mapped and has four-word blocks.
   - C2 is 4-way set-associative and has one-word blocks.

   If it matters to you, you may assume the computer uses 32-bit words and addresses and is byte-addressed (i.e., words are at addresses 0, 4, 8, etc.). Your explanations needn't be long.

   (a) If we want fewer compulsory misses than C0, should we use C1 or C2? Why?

   (b) If we want fewer conflict misses than C0, should we use C1 or C2? Why?

   (c) Which of C0 and C1 requires fewer total bits of storage? Why?

   (d) Which of C0 and C2 requires fewer total bits of storage? Why?

4. [**12 Points**] Suppose we want to design a system to handle 10,000 disk read requests per second. Each request is for a randomly located 4KB block on disk drives with the following specs:

   - 12,000 RPM rotational speed
   - 7 ms average seek time
   - 20 MB/s transfer rate.

   Assume there is no controller overhead or time spent running software in the processor. Assume also that the workload is spread evenly over 100 disk drives. Is this enough drives to deliver the desired performance? Justify your answer.

5. [**12 Points**] A multiprocessor system has a 750 MHz clock, and is running a program that has two phases:

   - Phase one is inherently sequential, running on only one processor no matter how many are available. This phase takes 10,000 instructions. Because these instructions are relatively simple, have good cache locality, etc., the average CPI for this phase is 1.
   - Phase two can be evenly divided over however many processors are available. This phase takes 100,000 instructions. Because these instructions are more complex and have more cache misses, the average CPI for this phase is 2.

   How many times faster is a 100-processor machine than a 10-processor machine? Assume there are no extra costs for communication or coordination. Show your work.