MCS284 Final Exam

Serial #:

This exam is open-book and mostly closed-notes. You may, however, use a single 8 1/2 by 11 sheet of paper with hand-written notes for reference. (Both sides of the sheet are OK.)

Please write your name only on this page. Do not turn the page until instructed, in order that everyone may have the same time. Then, be sure to look at all problems before deciding which one to do first. Some problems are easier than others, so plan your time accordingly. You have two hours to work.

Do only four of the five problems. If you do any work on all five, you must mark one of them "do not grade."

Write the answer to each problem on the page on which that problem appears. You may use the back of that same sheet if you need additional space. You may also request additional paper, which should be labeled with your test number and the problem number.

If any problem has a numerical answer, you are welcome to indicate the arithmetic that needs to be done rather than doing the arithmetic. For example, you could give as your answer $5 \times 12 + 3$ rather than 63. This will not result in any loss of credit.

If you are stuck, I am willing to sell you a hint for some points.

Name: _____

Problem	Page	Possible	Score
1	2	12	
2	3	12	
3	4	12	
4	5	12	
5	6	12	
Total		48	

1. [**12 Points**] Here is a sequence of address references given as word addresses: 1, 10, 0, 3, 10, 6, 11, 13. Assuming a direct-mapped cache with two-word blocks and a total size of 8 words, which references are hits and which are misses? Also show the final contents of the cache.

2. [**12 Points**] A byte-addressed machine has a 64 KB cache, which has a 16-byte block size and is also 2-way set associative.

   (a) How many bits of the address are used to select a byte within the block?

   (b) How many bytes of data can be stored in each set?

   (c) How many sets are there in the cache?

   (d) How many bits of the address are used to index a set?

   (e) If the address is 32 bits wide, how many bits is the tag field?

   (f) How many bits are used in each set for tag and valid bits?

3. [**12 Points**] Up to seven of the Seagate ST423451 drives described in Figure 8.6 on page 650 can be hooked to a single 20 MB/s Fast SCSI-2 I/O bus. Suppose the traffic to those drives consists of lots of independent reads of 8 KB blocks of data, where the data within each block is consecutively located on the disk, but each block is randomly located with respect to the preceding block. The traffic is uniformly spread across the drives. Is seven drives (the maximum number) enough to saturate the full 20 MB/s bandwidth of the bus? Justify your answer.

4. [**12 Points**] Suppose the software (both sending and receiving) for the ATM network on page 654 were made 10 times faster. What would the total host-to-host latency now be for a 1 KB message? Show your work.

5. [**12 Points**] A two-processor bus-based multiprocessor uses the coherence protocol shown on pages 722–724. Initially address A is in the invalid state in both processors' caches. Processor 2 reads from address A, then processor 2 write to it, then processor 1 writes to it, then processor 2 reads from it, then processor 1 reads from it, then processor 1 writes to it. These actions are shown in the following table, along with the initial states of address A in each cache. Fill in the remaining states.

cache 1 state	cache 2 state
invalid	invalid
processor 2 reads	
processor 2 writes	
processor 1 writes	
processor 2 reads	
processor 1 reads	
processor 1 writes	